Krassimir Markov, Vitalii Velychko, Oleksy Voloshin
(editors)

Information Models
of
Knowledge

ITHEA®

KIEV – SOFIA

2010

Krassimir Markov, Vitalii Velychko, Oleksy Voloshin (ed.)

Information Models of Knowledge

ITHEA®

Kiev, Ukraine – Sofia, Bulgaria, 2010

ISBN 978-954-16-0048-1

First edition

This book maintains articles on actual problems of research and application of information technologies, especially the new approaches, models, algorithms and methods fot information modeling of knowledge in: Intelligence metasynthesis and knowledge processing in intelligent systems; Formalisms and methods of knowledge representation; Connectionism and neural nets; System analysis and sintesis; Modelling of the complex artificial systems; Image Processing and Computer Vision; Computer virtual reality; Virtual laboratories for computer-aided design; Decision support systems; Information models of knowledge of and for education; Open social info-educational platforms; Web-based educational information systems; Semantic Web Technologies; Mathematical foundations for information modeling of knowledge; Discrete mathematics; Mathematical methods for research of complex systems.

It is represented that book articles will be interesting for experts in the field of information technologies as well as for practical users.

Printed in Ukraine

ISBN 978-954-16-0048-1

C\o Jusautor, Sofia, 2010

SIMPLE CONSTRAINED FOLDING OF PROGRAMMABLE LOGIC ARRAYS OF SPECIAL TYPE

Liudmila Cheremisinova, Irina Loginova

Abstract: *In the paper the constrained folding problem is investigated for programmable logic array (PLA) of special architecture type. Constraints applied to folding are given which are imposed by the used PLA structural features A PLA simple folding algorithm is presented which takes into account the PLA structure peculiarities.*

Keywords: *design automation, area optimization, PLA structure folding.*

ACM Classification Keywords: *B.6.3 [Logic Design]: Design Aids – Optimization; B.7.2 [Integrated circuits]: Design Aids –Layout.*

Conference topic: *Mathematical methods research of complex systems.*

Introduction

Structured logic refers to logic forms that exhibit a high degree of regularity in their layout and interconnections. One of widespread used regular structure is Programmable Logic Array (PLA) [Ullman, 1984]. The following are some of the reasons for wide use of PLA structures in chip design: they have regular structure that allows extensive use of automation in the design and routing and they are easy-to-modify. PLA is a popular, highly regular logic-structure and has a two-dimensional structure consisting of an array of rows and columns. There are transistors in intersections of some rows and columns. PLA layout design is easily automated because of its direct correspondence with PLA personality matrix. The price paid for the structural regularity is that much PLA area is unused because a large percentage of the row-column intersections are not personalized. Several techniques have been proposed for reducing the area required.

Existing PLA area minimization techniques can be divided into two categories: minimization of the functions being implemented without changing the input/output relationship, and restructuring the PLA matrix by reordering the rows and columns so that any empty space is eliminated. The first methods are concerned with two-level logic minimization of systems of Boolean functions [Brayton, 1984], [Zakrevskij, 2009] and the second ones with topological minimization of the PLA. Two-level logic minimization allows to reduce 1) the number of product terms and as the result the number of PLA rows, 2) the number of literals of product terms and as the result the number of transistors in PLA circuit, i.e. the PLA density.

Techniques of topological minimization reduce the number of physical columns and/or rows, they change the PLA structure by using a process called folding [Hachtel, 1982], [DeMicheli, 1983]. Folding is a technology-independent, it is developed for array structures and attempts to place two or more columns (and/or rows) together in the same physical vertical (and/or horizontal) line so that they can share this line. Column folding is said to be simple if utmost two columns (rows) share a single physical vertical (and/or horizontal) line. Otherwise, it is called multiple when more than two columns can share a single column.

Folding does not change the implemented logic in any manner, but reduces the number of columns (and/or rows), and thus reduces the area of the PLA. In the paper we deal with PLA folding and its effects on the PLA structure.

The peculiarities of topological implementation PLA structures of used type

The structure of a PLA is congruent with the sum-of-products representation of Boolean functions. The overall combinational PLA consists of a group of rows and columns and is characterized by number of inputs, outputs and product terms. It is a standard two level NOR-NOR structure that can be divided into two planes called the AND-plane and the OR-plane. For every input signal, there are two rows (columns) carrying uncomplement and complement input literals in the AND-plane. The literal row of a signal is connected to its complement via an inverter, and so they are situated in the neighborhood. For every output signal, there is a row (column) in the OR-

plane. The columns running across both planes correspond to product terms. PLA AND-plane produces the product terms which are used by the OR-plane to form the sum-of products (SOPs) of implemented functions.

Figures 1 and 2 show the physical layouts of two different PLA types. The first one is the traditional PLA that does not allow folding, and the second one that allows simple row folding. The both topological PLA structures implement the same SOP system with 8 input, 8 output variables and 13 product terms (PLA misex1 from Benchmark'91 set). The core of the both PLAs consists of AND and OR matrices having approximately the same sizes. The PLA structures differ in sizes of input buffers that are situated on the right and on the left from the AND matrix. Thus input signals feed input buffers from the both PLA sides.
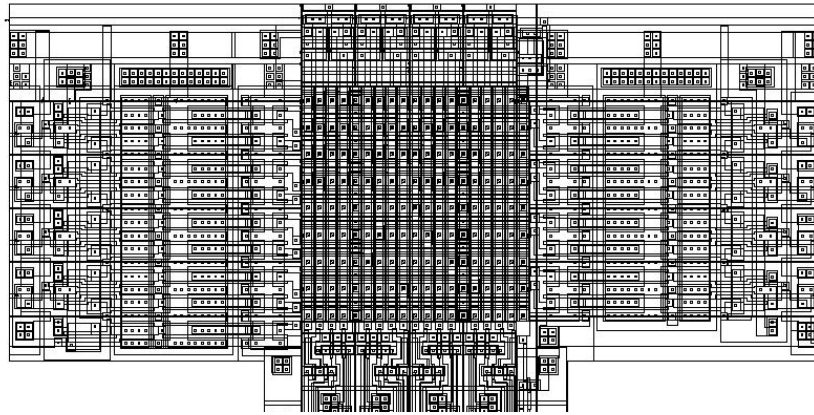

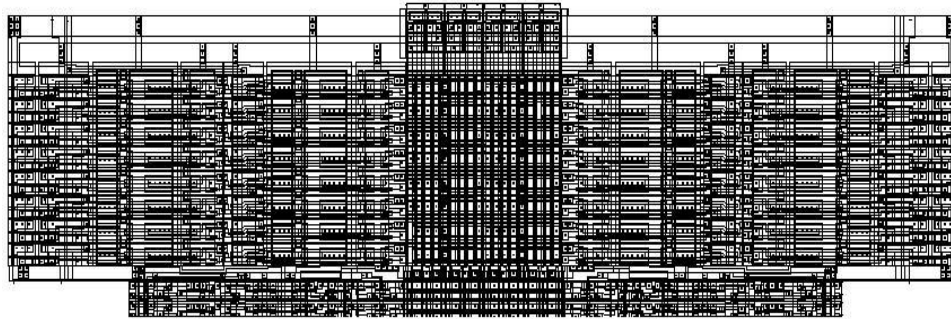Figure 1. Topological layout of AND-plane of the traditional PLA

Figure 2. Topological layout of AND-plane of the foldable PLA

Each row of PLA AND-plane consists of two horizontal lines currying signals corresponding to uncomplement and complement values of the same input variable. Each row of the traditional PLA (Figure 1) permits to be fed from the only PLA side. And a row of the foldable PLA (Figure 2) can take signals simultaneously from both PLA sides. In such a case these two signals share the same PLA row and such a manner we can realize PLA simple row folding. The same is true for the PLA OR-plane too, the matrix is not depicted in Figures 1 and 2 but it is organized in the same way.

From structural features of topological organization of foldable PLA structures some requirements follow. They must be taking into account when folding the PLA structure of foldable type.

1. Input signals corresponding to the literals x_i и $\overline{x_i}$ of the same variable enter transistor pins from the same input buffer, i.e. they occupy two neighboring horizontal lines of the same AND-plane row. It is allowed to place row

currying x_i above row currying $\bar{x}_i$ and vice versa, or to double some signals in the same PLA side or in the opposite side.

2. Each row of the PLA AND plane may be fed from both its sides when they can be folded each other. So two signals carrying x_i and $\bar{x}_i$ arrive, for instance, from the right and other signals carrying x_j and $\bar{x}_j$ arrive from the left. In this case the PLA line is divided into two segments separated from each other with the special break cell (in Figure 3 it is designated by a cross).
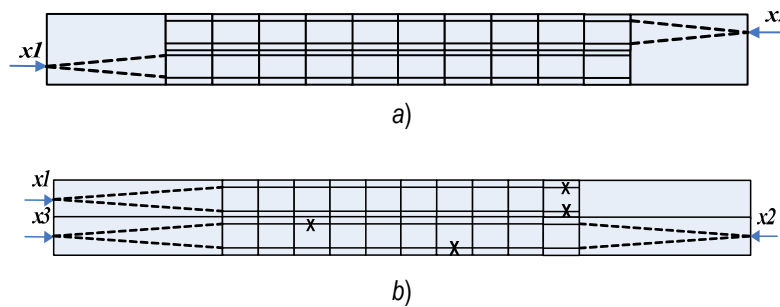

a)

b)

Figure 3. Sketch layout of the topology of rows of PLA AND-plane: a) for the case of traditional PLA; b) for the case of foldable PLA

3. When any variable does not participate in folding then it violates the other variable to feed from the opposite PLA side. To ensure blocking signal from the opposite PLA side the plug cell is introduced in this side.

4. In the case when one of the signals carrying x_i or $\bar{x}_i$ may be fed and the other is blocked with plug cell (both lines of this row are used for inputs from the other PLA side and one of the literals x_j or $\bar{x}_j$ is folded with x_i or $\bar{x}_i$) then one more row should be added for the feeding one of x_i or $\bar{x}_i$.

5. PLA of the considered type permits only simple row folding, i.e. only two external signals may share the same PLA line.

PLA-style logic structures and their folding

*In the folding problem either AND-plane or both AND- and OR-planes together are described in symbolic form by a Boolean matrix **B** having sets C(**B**) and R(**B**) of their columns (where uncomplement and complement modes of a variable have their own distinct column) and rows. 1 in the position i,j of the matrix **B** means there is an appropriate crosspoint (transistor) between the i-th row and the j-th column in the matrix. Each row ri $\in$ R(**B**) implies a set C(ri) $\subseteq$ C(**B**) of rows, which are populated on it:*

$c_j \in C(r_i) \leftrightarrow b^j_i = 1.$

The objective of the matrix folding is to find the maximum number of pairs of rows that can be folded (each pair can be merged into a single line) simultaneously.

Any two rows r_i and r_j are *disjoint* if

$C(r_i) \cap C(r_j) = \varnothing.$

Two disjoint rows do not have transistors on the same particular PLA row. If there are no restrictions on the folding type two disjoint rows are compatible and can be folded together, so they form a row *folding pair*.

The objective of matrix folding is to arrange the rows and columns of the initial matrix in the plane using the least number of rows by means of assigning rows to the same horizontal lines.

Row folding can be obtained by permuting the columns of the PLA, so it introduces a restriction on the order of the columns. Any ordered row folding pair (OFP) $<r_{k1},r_{k2}>$ can be actually implemented in the same horizontal PLA line moving r_{k1} to the left and r_{k2} to the right and resulting to permutation on the set of PLA columns: all

columns of $C(r_{k1})$ are at the left of those of $C(r_{k2})$. So OFP $p_k^o = <r_{k1},r_{k2}>$ induces a partial ordering $C(p_k^o)$: $C(r_{k1}) < C(r_{k2})$ upon the columns of $C(\mathbf{B})$, that is specified by Cartesian product $C(p_k^o) = C(r_{k1}) \times C(r_{k2})$. Any unordered column folding pair (FP) (r_{k1},r_{k2}) corresponds to two possible OFPs $<r_{k1},r_{k2}>$ or $<r_{k2},r_{k1}>$ and thus induces one of two possible partial ordering relationships.

Let we have, for example, a simple PLA structure whose AND-plane is described by the following Boolean matrix:

c_1	c_2	c_3	c_4	c_5	c_6	
1	1	0 0	0	0		a
0	0	1 0	0	1		$\bar{a}$
1	0	0 1	0	0		b
0	0	1	0	1	0	$\bar{b}$
0	0	0 1	0	0		c
1	0	1 0	1	0		$\bar{c}$
1	1	1 0	0	1		d
0	0	0 1	1	0		$\bar{d}$

$\mathbf{B} =$

For this PLA there are eight unordered row folding pairs:

$(a, \bar{b}), (a, c), (a, \bar{d}), (\bar{a}, b), (\bar{a}, c), (\bar{a}, \bar{d}), (\bar{b}, c), (c, d)$

or 16 ordered row folding pairs. OFP $p_{14}^o = <r_1,r_4> = <a, \bar{b}>$ induces the following partial ordering

$R(p_{14}^o) = R(r_1) \times R(r_4) = \{(c_1,c_3), (c_1,c_5), (c_2,c_3), (c_2,c_5)\}$.

A folding set (FS) $P = \{p_1, p_2, ..., p_s\}$ is a set of disjoint folding pairs (any row may enter only into one of pairs), and an ordered folding set (OFS) $P^o = \{p^o_1, p^o_2, ..., p^o_s\}$ is a set of disjoint ordered folding pairs. The relation $C(P^o)$ induced by OFS P^o is defined as being the union of the relations induced by OFPs belonging to OFS P^o. But the restrictions imposed on the order of columns by one set of folded rows might conflict with the column ordering desired by another set of folded rows. Such conflicts on column orderings along with some other conditions (explained in the next section), make row folding an NP-complete optimization problem [Hachtel, 1982].

In [Hachtel, 1982] it is said that the ordered folding set P^o is implementable (has no conflicts on column orderings) if the transitive closure of $\mathbf{C}_{P_o}{}^t$ of the ordering relation $\mathbf{C}_{P_o}$ is a partial ordering relation on $C(\mathbf{B})$. Partially ordered set of columns that corresponds to $\mathbf{C}_{P_o}$ can be embedded into a linearly ordered set of columns from $C(\mathbf{B})$. It is clear that implementable ordered folding set P^o contains all information needed to fold the matrix i.e. it specifies the pairs of rows to be folded together and their relative position (on the left or on the right). The objective is to find the implementable ordered folding set of maximum cardinality.

Thus folding requirements are as follows:

1) elements of a set of rows can be folded only if they are disjoint (there is no single column (product term) that uses both the rows (literals));

2) a set p_i of rows that can be folded should be compatible with a set P^o_t of rows that are already folded having in view that p_i should be compatible with respect to ordering of columns required by set P^o_t.

For example, the OFS $<r_2,r_8>$ defines a partial ordering relation $C_{2,8}$ of the mentioned matrix B:

$C_{2,8} = C(r_2) \times C(r_8) = \{(c_3,c_4), (c_3,c_5), (c_6,c_4), (c_6,c_5)\}$.

For the matrix B we can see that $P^o = \{<r_2,r_8>,<r_5,r_7>\}$ implies

$C'_{P_0} = C_{2,8} \cup C(r_5) \times C(r_7) = C_{2,8} \cup \{(c_4,c_1), (c_4,c_2), (c_4,c_3), (c_4,c_6)\}$.

Its transitive closure $C_{P_0}{}^t$ is not a partial ordering relation on $C(B)$ because there exist pairs (c_6,c_4) and (c_4,c_6). Thus $\{<r_2,r_8>,<r_5,r_7>\}$ is not implementable. In contradiction $\{<r_2,r_8>,<r_7,r_5>\}$ is implementable.

The peculiarities of folding of PLA structures of the considered type

As it was mentioned, the goal of simple row folding of PLA structures (without restrictions on the order of PLA columns and rows) is to find out an implementable ordered folding set of the greatest cardinality, i.e. having the most number of folding pairs. An ordered folding set P o = {po1, po2, …, pos} induces three-block partition (R1, R2, R3) of the set R(B) (and corresponding partition (X1, X2, X3) of the set of literals X): the rows of R1 and R2 are the left and right segments of ordered folding pairs poi $\in$ P o and all other rows are included in R3.

The analysis of peculiarities of topological architecture of PLA structures of the considered type shows that the following variants of implementation of folding pairs from ordered folding set P are available.

1. Isolated realization. Any variable x_i (and $\overline{x_i}$) occupies its own horizontal line (Figure 4, *a*) of the folded PLA if $x_i \in X_3$ and $\overline{x_i} \in X_3$. For instance a signal comes to the AND-plane from the left and the break cell is situated on the right hand side of the line.

2. Coupled realization of two folding pairs. When $<x_i^{\sigma}, x_j^{\rho}>$, $<x_i^{\sigma}, x_j^{\rho}> \in P^o$ ($\sigma,\rho \in \{0, 1\}$ and $x_i^1 = x_i$, $x_i^0 = \overline{x_i}$) then a distinct row (consisting of two horizontal lines) enters into AND-plane. It takes x_i and $\overline{x_i}$ on the left but x_j and $\overline{x_j}$ from the right (Figure 4, *b*). In this case compared with isolated realization (Figure 4, *a*), we have gain in PLA square equaled to one row or two lines.

3. Mixed realization. When $<x_i^{\sigma}, x_j^{\rho}> \in P^o$ but $x_i^{\sigma}, x_j^{\rho} \in X_3$ then the pair $<x_i^{\sigma}, x_j^{\rho}>$ is subject to elimination from P^o (with carrying x_i^{σ} and x_j^{ρ} into X_3) because the implementation of such a folding variant (Figure 4, *c*) does not give any gain in square in comparison with isolated realization of these two variables.

4. Combined realization. When $<x_i^{\sigma}, x_j^{\rho}> \in S$ and $<x_l^{\theta}, x_j^{\rho}> \in P^o$ (or $<x_j^{\rho}, x_l^{\theta}> \in P^o$, x_i^{σ} и x_l^{θ} are allowed to be or not to be in X_3) then PLA AND-plane has two rows fed by the same variable x_j (Figure 4, *d*). At the same time, the other two variables x_i and x_l take no additional PLA rows. In this case compared with isolated realization (Figure 4, *a*), we have gain in PLA square equaled to one row or two lines. But in comparison with coupled realization this gain should be divided on 3 (the number of participating variables) while in the case of the coupled realization it is divided on 2. As for combined realization, the variant when $x_i^{\overline{\sigma}}, x_l^{\overline{\theta}} \in X_3$ is more preferable as it allows to keep positive result of folding during topological implementation of folded PLA.

The purpose of row folding of PLA structure of considered type is to find out an implementable ordered folding set, not necessarily of the greatest cardinality, but providing the most gain in PLA square compared with not folded PLA. From the discussed above peculiarities of topological architecture of PLA structure it follows that the variant of coupled realization brings the most gain in comparison with the other variants, it provides saving 1 line per a variable. The second result is given by the combined realization, it provides saving 2/3 of line per a variable. The mixed realization as the variant of folding gives nothing compared with the isolated realization.
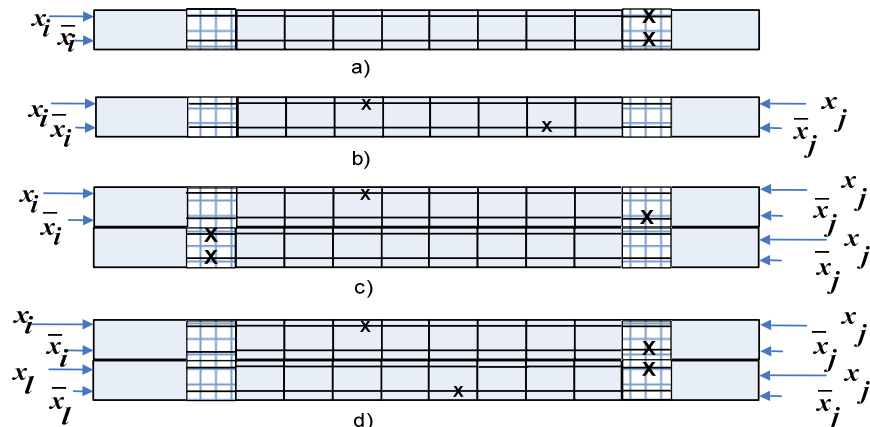
Figure 4. Sketch layouts of the variants of implementation of topology of PLA AND-plane rows

Having in view these reasons it is clear that the greatest reduction of PLA square can be achieved searching for implementable ordered folding set having as much as possible coupled folding pairs (variant 2) and, in the second turn, groups of combined three folding pairs (variant 4). The mixed realization (variant 3) gives nothing, so we may exclude from any ordered folding set each folding pair (r_{i1}, r_{i2}) corresponding to (x_i^σ, x_j^ρ) if $x_i^\sigma \in X_3$ and $x_j^\rho \in X_3$. Such pairs are "redundant" when searching for folding set of the most cardinality for PLA of considered type.

Method of simple row folding of PLA of considered type

A modification of the method [Cheremisinova, 1999] makes a good match for the PLA folding problem with discussed constraints on folding pairs. The method is based on the fact that implementable ordered folding set is a convex one: if an ordered folding set is implementable then any its subset is implementable too. The method supposes forming the compatibility relation on the set of folding pairs.

Taking into account that there is a great deal of folding pairs for rare PLA structures, here it is suggested to consider in initial stages of folding only unordered folding pairs. Any two unordered folding pairs (r_{i1}, r_{i2}) and (r_{j1}, r_{j2}) are compatible if unordered folding set (UFS) $\{(r_{i1}, r_{i2}), (r_{j1}, r_{j2})\}$ is implementable. And UFS $P = \{p_1, p_2, ..., p_s\}$ is implementable if there exist an ordering of unordered folding pairs $p_i \in P$ inducing implementable OFS $P^o = \{p^o_1, p^o_2, ..., p^o_s\}$.

In [Cheremisinova, 1999] it was shown that

1) if UFS P is implementable it consists of pairwise compatible folding pairs;

2) unordered folding pairs (r_{i1}, r_{i2}) and (r_{j1}, r_{j2}) are not compatible iff the following conditions take place:

$$1.\ C(r_{i1}) \cap C(r_{j2}) \neq \varnothing;$$
$$2.\ C(r_{i2}) \cap C(r_{j1}) \neq \varnothing;$$
$$3.\ C(r_{i1}) \cap C(r_{j1}) \neq \varnothing;$$
$$4.\ C(r_{i2}) \cap C(r_{j2}) \neq \varnothing.$$

(1)

If at least one of the conditions is violated the unordered folding pairs will be compatible.

The task of searching for PLA folding ensuring the most reduction of the area of PLA structure of considered type is broken into the following subgoals.

1. Searching for a set P^u of unordered folding pairs.

2. Excluding from P^u "redundant" folding pairs (as it is suggested in previous section).

*3. Forming the compatibility relation **S**p on the set P u of folding pairs.*

*4. Constructing a graph G = (V, E) of the compatibility relation **S**p where vertices from V correspond to the unordered folding pairs pi $\in$ P u and two vertices vi and vj are connected with an edge eij $\in$ E if corresponding pairs pi and pj are compatible.*

5. Searching for maximal cliques G_i = (V_i, E_i) of the graph G = (V, E).

6. Excluding from found cliques G_i = (V_i, E_i) vertices corresponding to "redundant" folding pairs (according to the folding pairs that are associated with the cliques).

7. Evaluating found maximal cliques G_i according to the criterion of saving of PLA lines (as in the previous section) and ordering the cliques G_i in accordance with these values.

8. Verifying whether unordered folding sets P_i^u corresponding to the cliques G_i are implementable and leaving out from further consideration cliques that violate this condition.

9. Choosing a clique G_i and the corresponding OFS of the most value of the criterion of saving PLA lines.

All the tasks except the tasks 5 and 8 have polynomial complexity, these two mentioned tasks are of exponential complexity.

*For the example considered above we have eight unordered row folding pairs: P u = {(a, $\overline{b}$), (a, c), (a, $\overline{d}$), ($\overline{a}$, b), ($\overline{a}$, c), ($\overline{a}$, $\overline{d}$), ($\overline{b}$, c), (c, d)}. So X3 = { $\overline{c}$ } and there are no "redundant" folding pairs in P ^{u} . Using (1) we define compatibility relation **S**$_p$ and then construct graph G = (V, E) of this relation shown in Figure 5.*

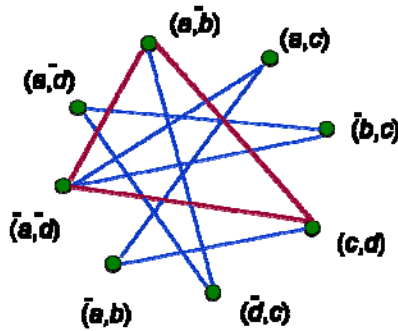Figure 5. Graph G = (V, E) of the compatibility relation

There exists the only maximal clique in the graph G = (V, E) having three vertices: (a, $\overline{b}$), ($\overline{a}$, $\overline{d}$), (c, d). For P^u = {(a, $\overline{b}$), ($\overline{a}$, $\overline{d}$), (c, d)} we get X3 = {b, $\overline{c}$} and establish that there is no "redundant" folding pairs in this P ^{u}. But as we have odd number of pairs, for the considered PLA type we can get gain only if we implement folding of two of them. So we should test on implementability two unordered folding sets: {(a, $\overline{b}$), ($\overline{a}$, $\overline{d}$)} and {($\overline{a}$, $\overline{d}$), (c, d)}, each of which has the same "binding" pair ($\overline{a}$, $\overline{d}$). Using the method [Cheremisinova, 2010] of checking whether the given sets of unordered folding pairs are implementable we determine that they are implementable and get two following implementable sets of ordered folding pairs:

$$\{< \overline{a}, \overline{d} >, < d, c >\}, \{< a, \overline{b} > < \overline{d}, \overline{a} >\}.$$

The implementations of these two ordered folding sets are shown in Figure 6 in diagram form.

In Figure 7 more complex example of folding task is considered. PLA description misex1 (Figure 7, *a*) from Benchmark'91 set is taken for folding. Its folded form is depicted in Figure 7, *b* where folding pairs are shown accompanied with the numbers of columns where break cells should be placed in the rows implementing folding pairs. Graphic form of implementation of the row folding is given in Figure 8.
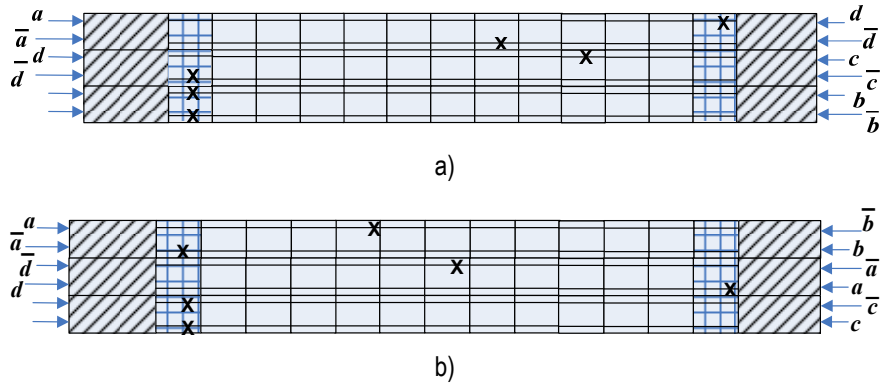
a)

b)

Figure 6. Sketch layouts of implementation of AND-plane columns from folding pairs:
a) {< $\bar{a}$, $\bar{d}$ >, < d, c >}; *b)* {< a, $\bar{b}$ > < $\bar{d}$, $\bar{a}$ >}

```
                      1
       13    8    8
      0111---- 10000100
      1010---- 10111001
      010----- 01011000
      1001---- 01011100
      0-00--1- 01011000
      001--1-- 01011000
      0011---- 01011000
      010----0 00100000
      01000--- 00100001
      0010-0-- 00110100
      01-1---- 00011000
      0000--0- 00010010
      0101---1 00000100
        IN
           a    ^a    b    ^b
           c    ^c    d    ^d
           e    ^e    f    ^f
           g    ^g    h    ^h
        OUT
           y0    y1    y2    y3
           y4    y5    y6    y7
      #####
      00000000
      #####
```

```
            13   19
            IN   11    5
             1    b          0
             2   ^b      g   9
             3          ^g   0
             4          ^f   0
             5    d      f   7
             6   ^d     ^h  11
             7    a      h   4
             8   ^a          0
             9   ^c          0
            10    c     ^e   9
            11          e    0
            OUT   8    0
             1   y0          0
             2   y1          0
             3   y2          0
             4   y3          0
             5   y4          0
             6   y5          0
             7   y6          0
             8   y7          0
            P
            #####
```

a)   *b)*

Figure 7. PLA misex1 folding: *a)* PLA misex1 description; *b)* description of the folded PLA
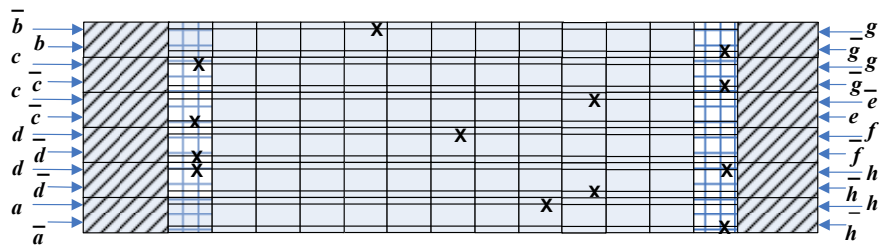

Figure 8. Sketch layout of implementation of topology of AND-plane rows of folded PLA misex1

Conclusion

The problem of reducing the area of the layout of PLA structures of a special type which allows row folding is investigated. The peculiarities of structural organization of this type PLA structures and its area optimization by means of folding are considered. Some restrictions imposed by the PLA topology on the folding mode are formulated. The task of PLA area optimization is formulated as constrained folding problem, and the method of simple row folding of PLA structures of considered type is proposed.

Acknowledgement

Bibliography

[Ullman, 1984] D. Jeffrey Ullman Computational aspects of VLSI. Rockville, Md.: Computer Science Press, 1984, 495 p.

[Brayton, 1984] R.K. Brayton, G.D. Hactel, C.T. McMullen et al. Logic minimization algorithm for VLSI synthesis. – Boston: Kluwer Academic Publishers, 1984, 193 p.

[Zakrevskij, 2009] A. Zakrevskij, Yu. Pottosin, L. Cheremisinova. Optimization in Boolean space. – Tallinn: TUT PRESS, 2009, 241 p.

[Hachtel, 1982] G.D. Hachtel, A.R. Newton and A.L. Sangiovanni-Vincentelli. An Algorithm for optimal PLA Folding. In: IEEE Trans. Computer-Aided Design of Integrated Circuit Syst., 1982, vol. CAD–1, No 2, pp. 63–77.

[DeMicheli, 1983] G. DeMicheli and A. Sangiovanni-Vincentelli. A. Multiple Constrained Folding of Programmable Logic Arrays: Theory and Applications. In: IEEE Trans. Computer-Aided Design, 1983, Vol. CAD-2, No 3, pp. 151–167.

[Cheremisinova, 1999] L.D. Cheremisinova. Some results in optimal PLA folding. In: Proc. of the Third Int. Conf. on Computer-Aided Design of Discrete Devices (CAD DD'99) (Minsk, Nov.10–12, 1999), 1999, Vol. 1, pp. 59–64.

[Cheremisinova, 2010] L. Cheremisinova. Multiple Folding of VLSI Regular Structure via Boolean Satisfiability. In: this issue.

Authors' Information

Liudmila Cheremisinova – *Principal Researcher, The United Institute of Informatics Problems of National Academy of Sciences of Belarus, Surganov str., 6, Minsk, 220012, Belarus, e-mail:* cld@newman.bas-net.by

Major Fields of Scientific Research: Logic Design, CAD systems, optimization

Irina Loginova – *Senior Researcher, The United Institute of Informatics Problems of National Academy of Sciences of Belarus, Surganov str., 6, Minsk, 220012, Belarus, e-mail:* cld@newman.bas-net.by

Major Fields of Scientific Research: Topological Design, CAD systems